4.7 A 4.5GHz LC-VCO with Self-Regulating Technique

Aleksander Dec[1], Ken Suyama[1], Tomomitsu Kitamura[2]

[1]Epoch Microelectronics, Hawthorne, NY
[2]Renesas Technology, Takasaki, Japan

The conventional approach for designing a low supply pushing VCO is to stabilize the supply voltage using a low-noise voltage regulator (Fig. 4.7.1). A bandgap reference is often used to generate a reference voltage that is insensitive to temperature and supply perturbations [1]. The bandgap reference voltage is then transformed to a desired regulated value by choosing an appropriate resistor divider ratio. The PMOS pass transistor is then sized sufficiently large so that it can source the required current while maintaining the loop gain. The output of the regulator provides the VCO with a supply voltage which is independent of temperature and external supply variations. Another dimension to the VCO design challenge is noise. The noise of the regulator is critical because it can seriously deteriorate the phase noise of the VCO. One approach to achieving a low-noise regulator, while keeping the current drawn by the regulator low, is to use large bypass capacitors to filter noise as well as provide stability (Fig. 4.7.1). However, it is not practical to integrate large capacitors on chip due to their large silicon area. Although these capacitors can be external to the chip, the current market trends force the reduction of external component count. Therefore, a fully integrated solution is strongly preferred. Another approach to achieve a sufficiently low-noise regulator is to minimize regulator noise by using a larger amount of bias current in the regulator. In particular, the noise generated by the bandgap voltage reference reduces as current through the bandgap core is increased. As a result, the core resistors are decreased and the multiple factor between diodes is increased. Although this is not a power-efficient approach, a sufficiently low-noise regulator with small area can be designed for the VCO in this way. To decrease the regulator noise until it is a nondominant noise contributor to the VCO phase noise, the current drawn by the regulator can be as large as the current drawn by the VCO.

Realizing that in some applications the bandgap core current and VCO core current may be of similar magnitude to meet the phase noise specifications, the same current can be shared by stacking VCO above the bandgap circuit as shown in Fig. 4.7.2. Only one opamp, which shares the function of amplifying the feedback error for the bandgap core and simultaneously creating a desired regulated voltage, is necessary. Thus, the circuit is merely a voltage regulator at DC, but an oscillator at AC. The bandgap core generates PTAT current (Q_3-Q_4, R_5-R_7). The cross-coupled NPN transistors (Q_1-Q_2) form V_{BE} multiplier to set up a desired regulated voltage for DC and at the same time provide AC positive feedback circuit for VCO core (Q_1-Q_2, C_{c2}). The inductors L_1 and L_2 are shorts at DC but form an LC tank with the AC-coupled varactors (C_{c1}, C_{v1}) and MIM-capacitor bank (C_{m0}, C_{m1}). The resistors R_1-R_7 are designed such that the regulated supply voltage is insensitive to temperature and external supply variations. The emitters of V_{BE} multipliers (Q_1-Q_2) are at the small-signal ground, and therefore oscillations do not affect the regulator.

This technique has several advantages. First, the current that is necessary to make the VCO oscillate is used to regulate the VCO supply voltage. Therefore, the regulator current is eliminated. Second, no external capacitors are needed for lowering regulator noise. This reduces the pin count of the chip. Third, the regulating amplifier in Fig. 4.7.1 is eliminated. The bandgap error correcting amplifier is also acting as the error amplifier for the DC regulation. Therefore, the chip area and current used by of this amplifier are eliminated. Fourth, this VCO achieves low supply pushing since it is regulating itself. Fifth, the negative resistance of the VCO is constant over temperature and supply variations due to PTAT bias current. This ensures reliable oscillation over temperature variations. Sixth, the oscillation amplitude increases with temperature but stays constant over supply variations. This slightly improves the phase noise improve as the temperature increases [2]. The self-regulating scheme can also be extended to CMOS VCOs.

A test chip for a 4.5GHz LC-VCO using the self-regulating technique is designed using a 0.18µm SOI BiCMOS process with 5 aluminum layers. Tuning is done through a binary weighted 6b MIM capacitor array for coarse tuning and a PN junction varactors for fine tuning. A center-tap spiral inductor (L=0.38nH, one-side) was designed using ASITIC [3]. The external nominal supply voltage is 2.8 V while the regulated voltage is designed to be 2.5V. The chip is packaged in a standard QFN48 package. All measurements are done using an Agilent 8452B VCO/PLL Signal Analyzer. The frequency coverage is 4.1GHz to 5.1GHz (Fig. 4.7.3). The worst-case supply pushing is 80kHz/0.1V (Figure 4.7.4). The current draw is 1.8 mA for all tuning combinations. The phase noise at 1MHz offset frequency is nominally –116dBc/Hz and varies by ±2dB for the lowest, middle, and highest bands with different tuning voltage settings (Fig. 4.7.5). Phase noise improves slightly with temperature as expected (Fig. 4.7.6). The achieved phase noise is sufficient for applications such as Zigbee and WCDMA. The chip micrograph is shown in Fig. 4.7.7. The entire self-regulated VCO occupies an area of $450\times600\mu m^2$.

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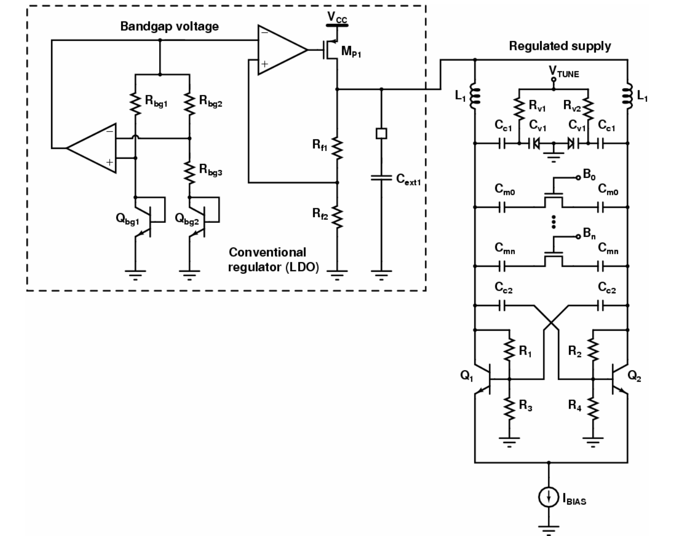

Figure 4.7.1: Conventional approach to regulate a VCO supply voltage to reduce the supply pushing of an LC VCO.

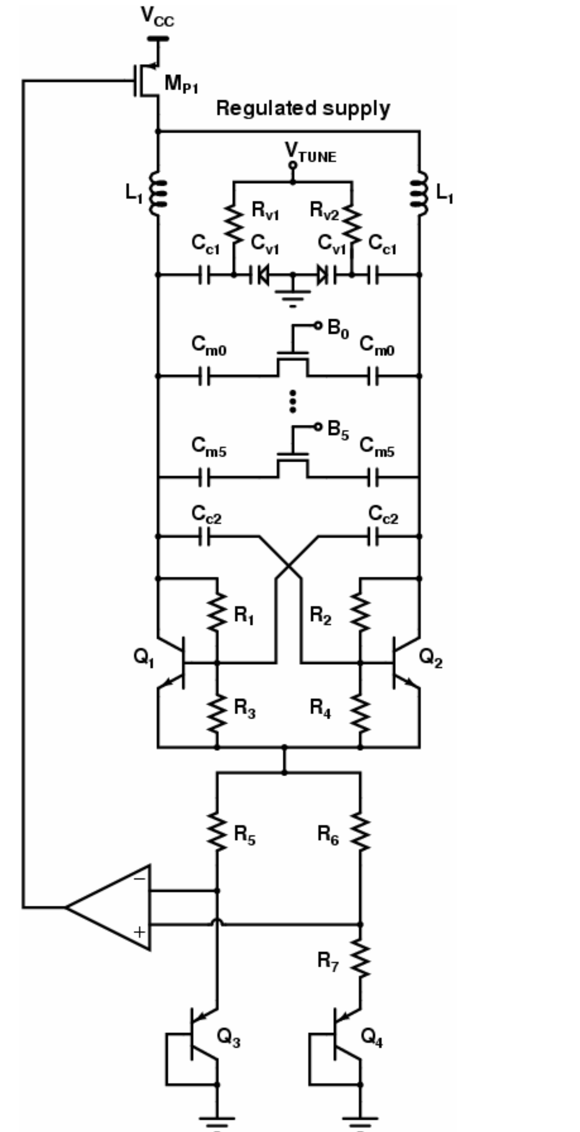

Figure 4.7.2: Simplified schematic of the proposed self-regulated LC VCO (the start-up circuit is not shown).

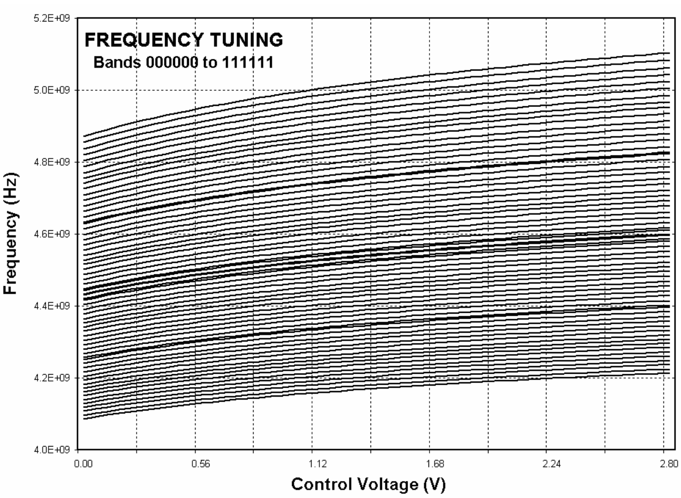

Figure 4.7.3: Measured frequency tuning characteristics.

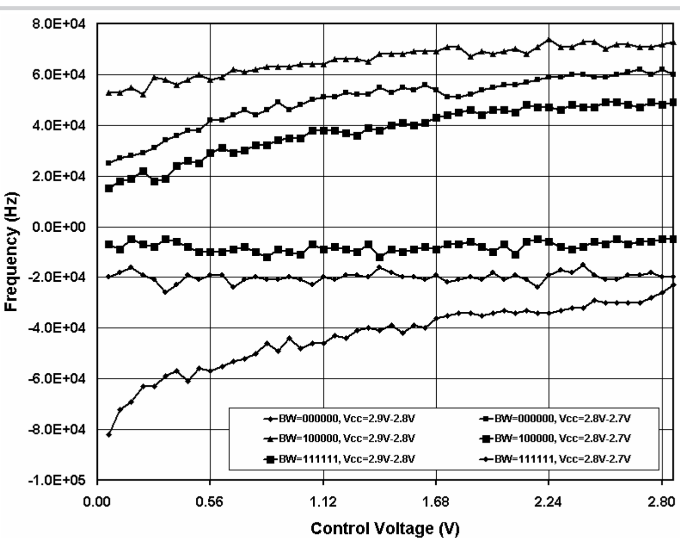

Figure 4.7.4: Supply pushing over control voltage for V_{cc}= 2.8V±0.1V and for the lowest, middle, and highest bands.

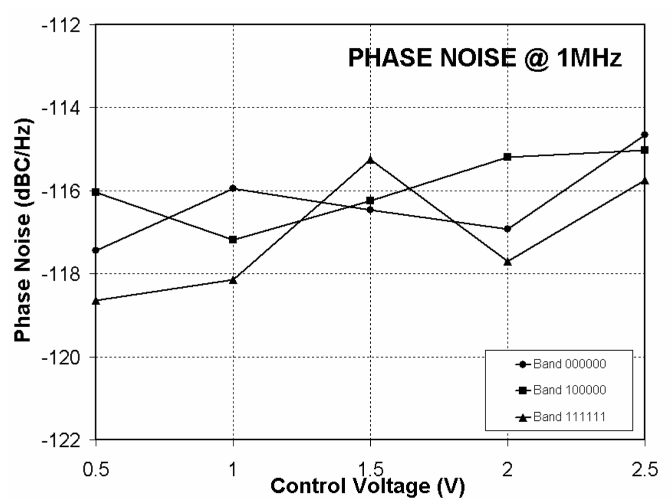

Figure 4.7.5: The phase noise performance at 1MHz offset at room temperature for the lowest, middle, and highest bands for different tuning voltages.

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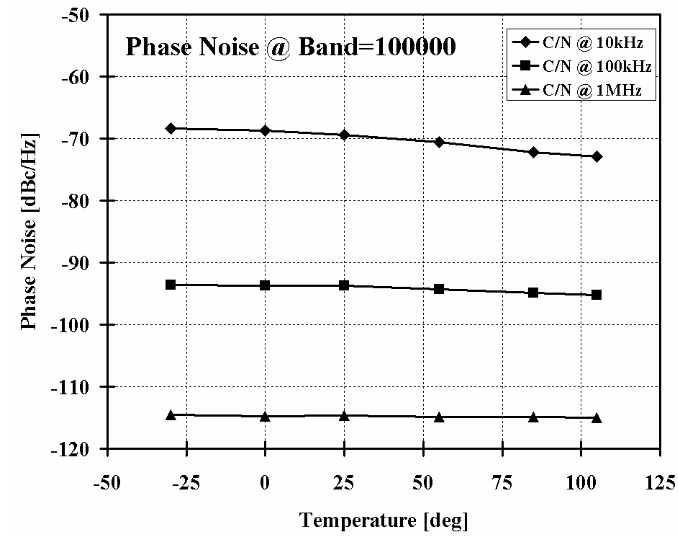

Figure 4.7.6: The phase noise performance at 10kHz, 100kHz, and 1MHz over temperature for the middle band.

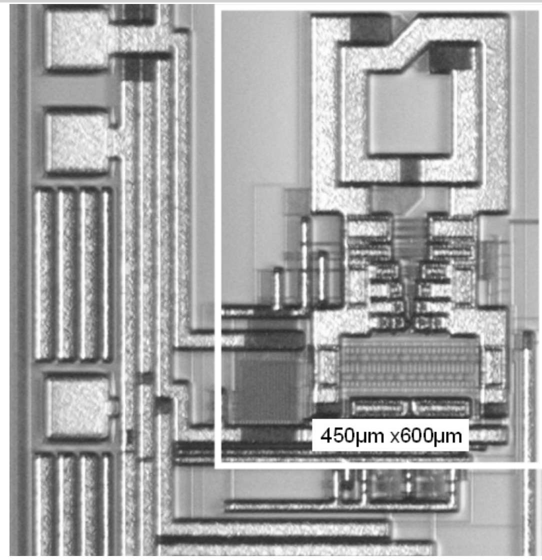

Figure 4.7.7: Chip micrograph.

